



Faculty of Technology  
University of Delhi



### About Faculty of Technology (FoT)

The Faculty of Technology (FoT) at the University of Delhi, North Campus, is a newly established and rapidly growing academic unit dedicated to advancing excellence in engineering and technology education. It presently offers B.Tech. programmes in Computer Science and Engineering (CSE), Electronics and Communication Engineering (ECE), and Electrical Engineering (EE) under the framework of the National Education Policy (NEP)-2020.

The Faculty of Technology builds upon the illustrious engineering legacy of the University of Delhi, which earlier nurtured renowned institutions such as Delhi Technological University (Formerly Delhi College of Engineering) and Netaji Subhas University of Technology (Formerly NSIT) before they became autonomous universities.

Situated in the vibrant North Campus of DU, the Faculty is envisioned as a multidisciplinary hub that integrates teaching, research, and innovation in emerging technological domains. The curriculum emphasizes industry linkage, experiential learning, and societal impact, aligning with the nation's vision of Atmanirbhar Bharat and sustainable technological growth.

### About FDP

The Faculty Development Programme (FDP) on “Advanced VLSI Design and Verification using Cadence EDA Tools” aims to provide participants with comprehensive exposure to the complete IC design and verification flow. The program covers RTL design, synthesis, floorplanning, placement, routing, physical verification, and post-layout simulation using tools such as Virtuoso, Genus, Innovus, and Spectre. Conducted by experts from Entuple Technologies Pvt. Ltd., the FDP emphasizes timing, power, and functional verification at advanced technology nodes. Through expert lectures and hands-on lab sessions, participants will gain practical insights into SoC design, verification methodologies, and tape-out readiness.

### Topics to be Covered

- Introduction to Full Custom IC Design Flow
- Cadence Solutions for Custom IC Design
- Schematic Capture using Virtuoso Schematic Editor
- Testbench Creation using Virtuoso Schematic Editor
- Functional Simulation using Spectre
- Layout Design using Virtuoso Layout Editor
- Parasitic Extraction using Quantus
- Post Layout Simulation
- Generation of GDSII

*Lab Sessions and Tutorials will be only for the shortlisted candidates at Room 303, Maharishi Kanad Bhawan, North Campus, University of Delhi, Delhi - 110007*

### Registration Details

Registration Link:

[Click here to register](#)

Or

Scan to register:



**There is no registration fee. However, certificates will be awarded only to participants who successfully attend all the sessions.**

One-Week

## Faculty Development Program

on

**“Advanced VLSI Design and Verification using Cadence EDA Tools”**  
from

**10<sup>th</sup> to 14<sup>th</sup> November’ 2025**

Organised by

**Faculty of Technology,  
University of Delhi**

In Collaboration with

**Entuple Technologies Pvt. Ltd.**



Faculty of Technology  
University of Delhi



**Prof. Sanjeev Singh**  
Dean, FoT, DU

**Dr. Vanita Jain**  
Associate Professor, FoT  
(Convener)

**Dr. Jeetendra Prasad**  
Assistant Professor, FoT  
(Co-Convener)

**Ms. Geetanjali Bhola**  
Assistant Professor, FoT  
(Co-Convener)

### Important Dates:

Registration starts on: 17<sup>th</sup> October, 2025

Last Date to register: 7<sup>th</sup> November, 2025; 11:59PM

### Note:

- No TA/DA or accommodation will be provided. Participants are requested to make their own arrangements
- 40 Seats for Faculty/Research Scholars.
- **Mode: Offline**



| TECHNOLOGIES |                                     |                                                     |                                                   |                                                    |                                                    |                                                   |                     |                                                    |                                     |                  |                  |
|--------------|-------------------------------------|-----------------------------------------------------|---------------------------------------------------|----------------------------------------------------|----------------------------------------------------|---------------------------------------------------|---------------------|----------------------------------------------------|-------------------------------------|------------------|------------------|
| Day-1        | Session-1:<br>(10:00 AM - 01:00 PM) | Inauguration ceremony                               | Tea Break                                         | Introduction to Full Custom IC Design Flow         | Cadence Solutions for Custom IC Design             | Schematic Capture using Virtuoso Schematic Editor | Symbol Creation     | Testbench Creation using Virtuoso Schematic Editor | Functional Simulation using Spectre | Delay Estimation | Power estimation |
|              | Session-2:<br>(02:00 PM - 04:00 PM) | Layout Design using Virtuoso Layout Editor          | Physical Verification which includes DRC & LVS    | Parasitic Extraction using Quantus                 | Post Layout Simulation                             | Area Estimation                                   | Generation of GDSII |                                                    |                                     |                  |                  |
| Day-2        | Session-1:<br>(10:00 AM - 01:00 PM) | Introduction to FinFET Library model                | Schematic Capture using Virtuoso Schematic Editor | Symbol Creation                                    | Testbench Creation using Virtuoso Schematic Editor | Functional Simulation using Spectre               | Delay Estimation    |                                                    | Power estimation                    |                  |                  |
|              | Session-2:<br>(02:00 PM - 04:00 PM) | Layout Design using Virtuoso Layout Editor          | Physical Verification which includes DRC & LVS    | Area Estimation                                    | Generation of GDSII                                |                                                   |                     |                                                    |                                     |                  |                  |
| Day-3        | Session-1:<br>(10:00 AM - 01:00 PM) | Introduction to Semi Custom IC Design Flow          | Cadence Solutions for Semi Custom IC Design       | Functional Verification using INCISIVE             | RTL Synthesis using GENUS Synthesis Solution       | Reports Generation (Power, Timing and Area)       |                     |                                                    |                                     |                  |                  |
|              | Session-2:<br>(02:00 PM - 04:00 PM) | Physical Implementation using INNOVUS that includes | FLOOR PLANNING                                    | POWER PLANNING                                     | PLACEMENT                                          | CTS                                               | ROUTING             | Generation of GDSII                                |                                     |                  |                  |
| Day-4        | Session-1:<br>(10:00 AM - 01:00 PM) | Introduction to STA Flow                            | Cadence Solutions for Static Timing Analysis      | Static Timing Analysis by using Innovus and Tempus | Introduction to AMS Design Flow                    |                                                   |                     |                                                    |                                     |                  |                  |
|              | Session-2:<br>(02:00 PM - 04:00 PM) | Introduction to AMS Design Flow                     | Cadence Solutions for Analog and Mixed Design     | Functional Simulation Using Spectre                |                                                    |                                                   |                     |                                                    |                                     |                  |                  |
| Day-5        | Session-1:<br>(10:00 AM - 01:00 PM) | Introduction to Functional Verification             |                                                   | Functional Verification using Conformal LEC Tool   |                                                    | Pre & Post Synthesis Analysis                     |                     |                                                    |                                     |                  |                  |
|              | Session-2:<br>(02:00 PM - 04:00 PM) | Introduction to DFT (Design For Test)               | Synthesis based on DFT using Modus tool           | ATPG Based DFT                                     | Valedictory Ceremony and certificate distribution  |                                                   |                     |                                                    |                                     |                  |                  |