ONE-WEEK OFFLINE

Faculty Development Program

ON

"Advanced VLSI Design and Verification using Cadence EDA Tools"

FROM 12th to 16th January,2026

Organised by

Faculty of Technology
University of Delhi

In Collaboration with

Entuple Technologies Pvt. Ltd.

Registration Details

Scan to register

Registration starts on : 17 December, 2025

Last Date to register : 5 January, 2026; 11:59PM

There is no registration fee. However, certificates will be awarded only to participants who successfully attend all the sessions.

Note :

- No TA/DA or accommodation will be provided. Participants are requested to make their own arrangements.
- Only 40 Seats for Faculty/Research Scholars
- Mode: Offline

Prof. Sanjeev Singh
Dean, FoT, DU

Prof. Vanita Jain
FoT, DU
(Convener)

Dr. Jeetendra Prasad
Assistant Professor, FoT
(Coordinator)

Ms. Geetanjali Bhola
Assistant Professor, FoT
(Coordinator)